# EKALAVYA
## The EC LAB

VEDHYA TECHNOLOGIES®
Breakthrough innovations

A convenient and cost-effective pocket HDL platform for every aspiring Engineer in

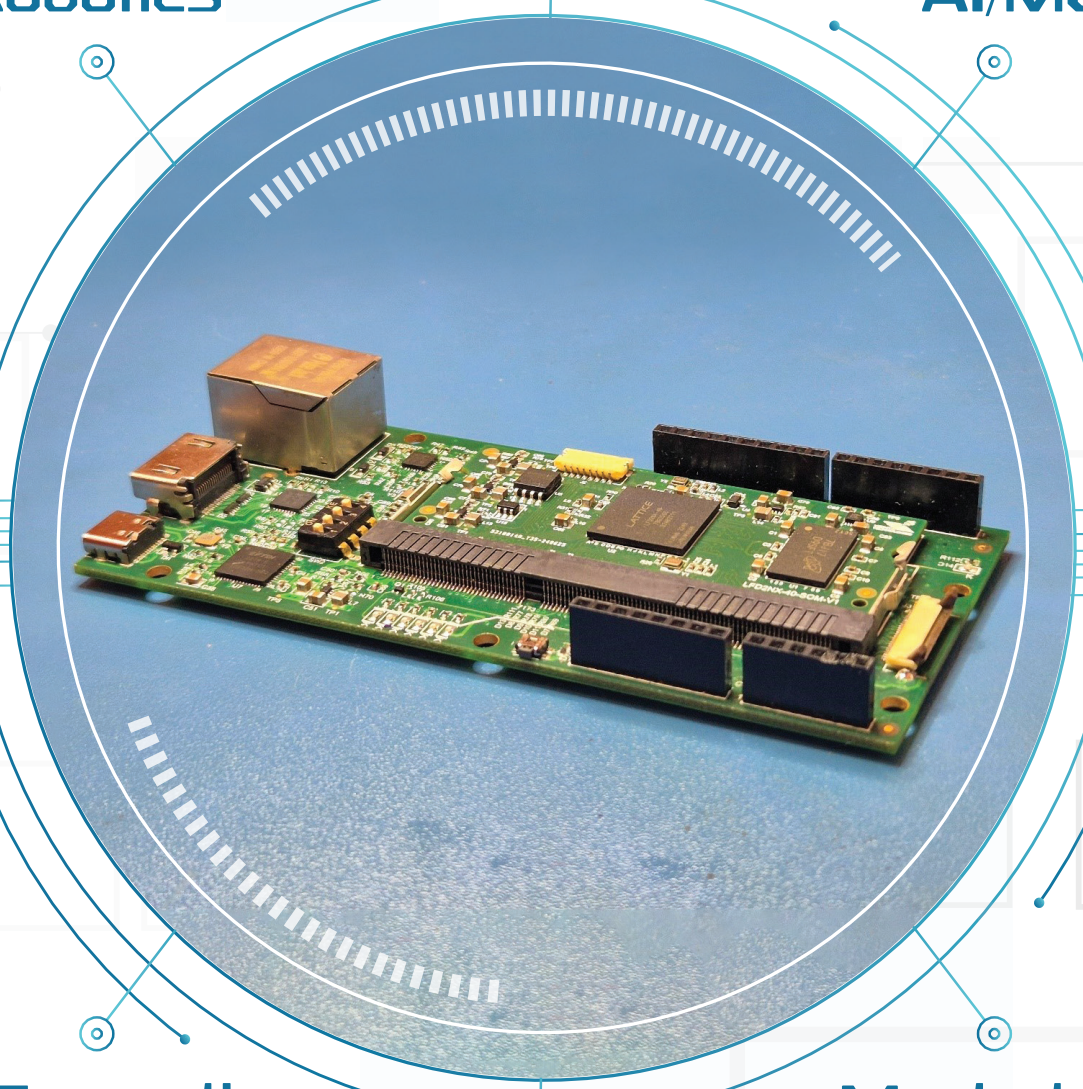
## Embedded Electronic Design

Enables fundamental building blocks for applications in

Electronic Engineering

Robotics

AI/ML



Edge Computing

Mechatronics

Industrial Automation

## The LAKSHYA of EKALAVYA

With the ever-increasing complexity of modern electronic systems and the demand for efficient, reliable, and scalable design methodologies there arises a compelling need for FPGA driven edge computing systems propelled by Hardware Description Languages (HDL) in digital electronics.

The need to build fundamental building blocks for varied applications and making engineering students industry ready necessitated the genesis of **EKALAVYA – The EC Lab.**

Our objective is to enable every electronic engineering /VLSI student to own and enable EKALAVYA – the pocket EC Lab for achieving Atmanirbhar as they take on industry roles.

**EKALAVYA** is an open-source RISC V/ ARM Cortex, AI enabled HDL platform that provides seamless implementation with wide range of Arduino compatible plugins using VHDL/Verilog.

Engineering students with this Pocket Lab and in combination of various compatible boards will have the opportunity to conduct a wide array of available experiments based on their current syllabus from the 1st to the 8th Semester. Those students having an additional appetite for up skilling themselves with hands on experiments/capabilities in areas of Edge computing for AI, ML, Mechatronics, Robotics and Industrial Automation to name a few, can choose the appropriate compatible board which in combination with the main EC Lab unit will fuel their innovative spark, enable their project initiatives and overall empower them to be better industry prepared. The above flexibility to use varied compatible boards can be a Gateway to build edge computing modules.

## Why is HDL going to play a pivotal role in digital electronics design and development?

A few advantages to name a few are abstraction and flexibility, Efficient workflow, Speed and efficiency, Scalability and reusability, Portability across platforms, Automation and tool integration, Simulation, Testing and verification, Rapid prototyping, Parallelism in digital Systems, Cost and time efficiency.

## Ekalavya architecture
## From an AI / ML perspective

- Well integrated into the TensorFlow and TensorFlow Lite framework providing superior ease of use over legacy and alternative platforms.
- Extends upon TensorFlow's extensive software development environment by generating all the necessary firmware to deploy a machine learning model directly onto FPGAs.
- Is a Machine Learning development platform to deploy Convolutional Neural Networks (CNN) on FPGAs, it includes software scripts needed to convert TensorFlow files and accelerator FPGA IP.

## From a VLSI perspective

In VLSI, a HDL like Verilog or VHDL is used to describe the behaviour and structure of digital circuits and systems, allowing engineers to design, simulate, and verify complex integrated circuits using a high-level language before physically implementing them on silicon; essentially acting as a blueprint for the hardware design, enabling efficient design, optimization, and validation processes.

HDL used as a VLSI programming language is independent of technology—you can implement the design using any technology. It is easy to design and troubleshoot any bugs in HDL. HDLs are so user-friendly to design large complex ICs that schematics are not drawn for such designs.

Key points about using HDL in VLSI: Design representation, Simulation, synthesis, Verification and improved efficiency it can be used to design and validate the customised ASIC and micro-controllers which find use in objects of daily use as well as complex scientific instruments. Fully supports Windows and Linux including Ubuntu.

## Salient Features

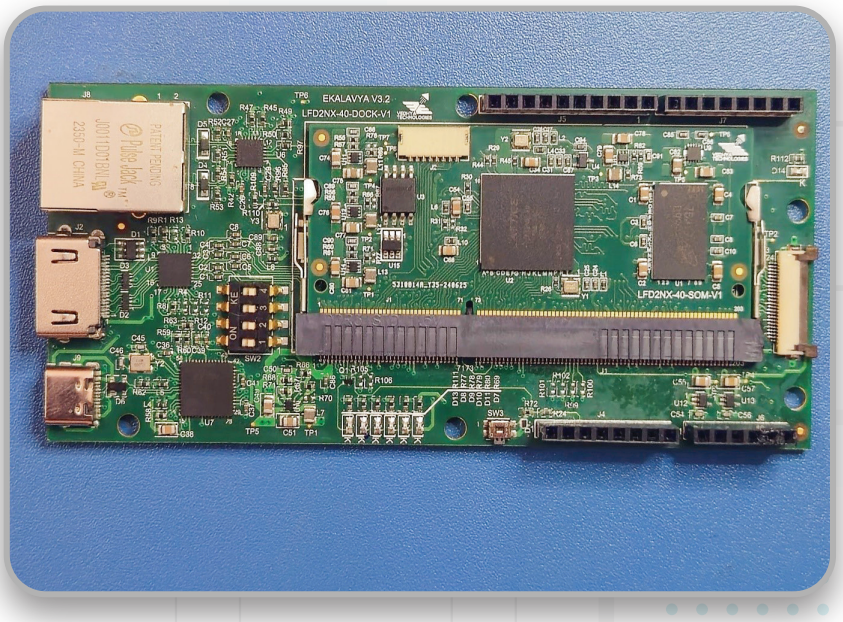
- Built-in IP support for wide range of Sensor for Quick development of Algorithms that can be implemented.
- Robust IP Library for building applications for AI or ML.
- Designed to work with applications across verticals through specific breakout boards covering utmost IO.
- User-friendly IDE that works on both Windows and Linux.

## Benefits

- Breaking down complex digital designs.
- Enable Cortex M1 / RISV32V architecture.
- Scalable and Affordable based on student's drive to learn.
- Simple and clear programming environment that supports creation of own microprocessor.
- Industry aspirants to get hands on in working on various experiments/capability options using the VHDL / Verilog environment.

## Ekalavya- The EC Lab
## FPGA features:

- Logic Cells 39000
- Logic units(LUT4) 32256
- Registers 32256
- Embedded Memory (EBR) Blocks 84
- EBR bits(kb) 1512
- Numbers of LRAM 2
- Large Memory (LRAM) Bits (kb) 1024
- Numbers of 18 X 18 Multipliers 56
- ADC Blocks 2
- Numbers of 18x18 Multiplier 56
- Numbers of PLLs 3
- Numbers of DLLs 2
- 5 Gb/s PCIe Gen2 Hard IP 1
- I/O Bank 8 Banks
- Root of Trust
- ECDSA bitstream authentication, coupled with robust AES-256 encryption.
- Migration path to PQC



**Indicative experiments in various domains using varied Arduino compatible boards in conjunction with the EC Lab using VHDL / Verilog**

## 1. ELECTRONIC ENGINEERING

### Basic Digital Electronic Experiments

- Logic Gates (NOR/AND/NAND/XOR/OR).
- Half Adder and Full Adder.
- Shift Register.
- FSM using Moore and Mealy.
- Arithmetic Logic Unit.
- UP/DOWN counters.
- Interface with sensors like temperature, humidity etc.

## 2. MECHATRONICS

### Discrete IO capability experiments

- DC Motor Control.
- Encoder Interface.
- Customized PLC Block.
- Driver Control Circuit for Stepper Motor.
- Analog to Digital Converters.
- Drive Pneumatic Valves.
- Interface Sensor with Discrete / Analog input.
- Interface with Discrete /Analog control (Servo Motors).

## 3. SIGNAL PROCESSING

### Data Acquisition capability experiments

- FIR Circuits.
- Fixed Floating-point Addition and multiplication.
- Low Pass and High Pass Filters.
- FFT.
- DDS (Digital Direct Synthesis).

## 4. AI & ML

### Image Processing Capability experiments using onboard HDMI and MIPI Camera interface

- Customised Algorithms implementation.
- HDMI/DVI Input Designs for Object detection.
- Audio Input Designs for Speech and Sound Detection.
- Camera Input Designs for Object Detection.

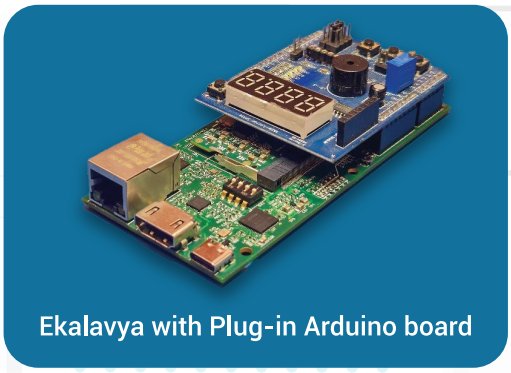
## 5. COMMUNICATION

### Protocols using Standard Arduino Plug-in boards

- UART application.
- I2C application.
- SPI application.
- Socket programming application (Wired/Wireless).
- MODBUS protocol.
- Cloud application.

## Online Community Forum

Vedhya Technologies will have an online presence through blogs, social media and online community forum to share thoughts and collaborate on ideas. It will look to guide aspirants to provide any clarification on concepts, programming and Interface issues on both Verilog and VHDL. One needs to register the product on **www.vedhyatech.com** in order to get access to the various platform upgrades, new releases and interact with industry experts. The forum aims to share insights resulting out of continuous feedback and SME opinions on industry trends and innovations



Ekalavya with Plug-in Arduino board

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